CLAIMS

Please cancel claims 19-26 without prejudice or disclaimer, and please amend the claims and add new claims as shown in the following claim listing.

1. (Currently amended) A system comprising:

a bus having a plurality of lines;

a first device having a first transmitter ~~connected to the bus and configured~~ to transmit ~~a~~ first ~~signal~~signals in a first frequency band over one line of the bus ~~in a first frequency band~~ and having a receiver to receive second signals in a second frequency band over the one line of the bus while first signals are transmitted over the one line of the bus; and

a second device to communicate with the first device over the bus, the second device having a second transmitter ~~connected to the bus and configured~~ to transmit ~~a~~ second ~~signal~~signals in the second frequency band over the one line of the bus ~~in a second frequency band at the same time that the first transmitter is transmitting the first signal;~~,

~~a first receiver connected to the bus and configured to receive the first signal transmitted over the bus in the first frequency band; and~~

~~a second receiver connected to the bus and configured to receive the second signal transmitted over the bus in the second frequency band,~~

wherein the first frequency band and the second frequency band occupy different portions of ~~the~~a frequency spectrum.

2. (Currently amended) The system of claim 1 wherein the first transmitter includes a ~~first~~ filter having a ~~first~~ cutoff frequency ~~defining~~to define at least in part the first frequency band.

3. (Currently amended) The system of claim 1 wherein the first transmitter includes ~~a~~ ~~first~~an encoder ~~defining~~to define at least in part the first frequency band.

4. (Currently amended) The system of claim 3 wherein the ~~first~~ encoder has a defined ~~first~~ run length ~~defining at least in part the first frequency band~~.

5. (Currently amended) The system of claim 3 wherein the ~~first~~ encoder comprises a combinational logic table.

6. (Currently amended) The system of claim 1 wherein the first transmitter and the ~~second~~ receiver are part of a single chip.

7. (Original) The system of claim 1 wherein the first frequency band and the second frequency band are fixed.

8. (Currently amended) The system of claim 1 ~~further~~ comprising a band setting unit ~~configured~~ to set the first frequency band and the second frequency band in response to an input signal.

9. (Currently amended) The system of claim 8 ~~further~~ comprising a user selection device ~~configured~~ to generate the input signal.

10. (Currently amended) The system of claim 8 ~~further~~ comprising a first arbitration module and a second arbitration module ~~configured~~ to arbitrate between one another to generate the input signal.

11. (Currently amended) The system of claim 1 wherein the first transmitter and the ~~second~~ receiver are associated with a microprocessor.

12. (Currently amended) The system of claim 1 wherein the first transmitter and the ~~second~~ receiver are associated with a memory storage device.

13. (Currently amended) The system of claim 1 wherein the first transmitter and the ~~second~~ receiver are associated with a chipset.

14. (Currently amended) The system of claim 1 wherein:

the first transmitter includes a first output connected to the one line of the bus;

the second transmitter includes a second output connected to the one line of the bus; and

the ~~first~~ receiver includes ~~a first~~an input connected to the one line of the bus~~; and~~

~~the second receiver includes a second input connected to the bus~~.

15. (Currently amended) A ~~microprocessor~~ device comprising:

a transmitter ~~configured~~ to transmit ~~a~~ first ~~signal~~signals in a first frequency band over one of a plurality of lines of a bus over which the device is to communicate with another device~~in a first frequency band; and~~

a receiver ~~configured~~ to receive ~~a~~ second ~~signal~~signals in a second frequency band ~~simultaneously transmitted~~ over the one line of the bus ~~in a second frequency band~~while first signals are transmitted over the one line of the bus,

wherein the first frequency band and the second frequency band occupy different portions of ~~the~~a frequency spectrum; and

a functional portion to transmit signals using the transmitter and to receive signals using the receiver.

16. (Currently amended) The ~~microprocessor~~ device of claim 15 wherein the transmitter includes a ~~first~~ filter having a ~~first~~ cutoff frequency ~~defining~~to define at least in part the first frequency band.

17. (Currently amended) The ~~microprocessor~~ device of claim 15 wherein the transmitter includes ~~a first~~an encoder ~~defining~~to define at least in part the first frequency band.

18. (Currently amended) The ~~microprocessor~~ device of claim 15 wherein the first frequency band and the second frequency band are fixed.

19. (Canceled).

20. (Canceled).

21. (Canceled).

22. (Canceled).

23. (Canceled).

24. (Canceled).

25. (Canceled).

26. (Canceled).

27. (Currently amended) A method ~~of transmitting data within a device,~~ comprising:

transmitting by a first device ~~a~~ first ~~signal~~signals ~~over a bus~~ in a first frequency band over one of a plurality of lines of a bus over which the first device is to communicate with a second device; and

~~transmitting a second signal over the bus in a second frequency band;~~

~~receiving the first signal transmitted over the bus; and~~

receiving by the first device ~~the~~ second ~~signal~~signals in a second frequency band ~~transmitted~~ over the one line of the bus while first signals are transmitted over the one line of the bus,

wherein~~:~~ the first frequency band and the second frequency band occupy different portions of ~~the~~a frequency spectrum~~; and~~

~~transmitting the first signal, transmitting the second signal, receiving the first signal, and receiving the second signal all occur simultaneously~~.

28. (Currently amended) The method of claim 27 wherein transmitting ~~the~~ first ~~signal~~signals includes encoding an output to form ~~the~~a first signal in the first frequency band.

29. (Currently amended) The method of claim 28 wherein transmitting ~~the~~ first ~~signal~~signals includes encoding an output to form ~~the~~a first signal with a defined ~~first~~ run length.

30. (Currently amended) The method of claim 27 ~~further~~ comprising setting ~~a spectral band of~~ the first frequency band and the second frequency band ~~based upon a set signal~~.

31. (Currently amended) The method of claim 30 ~~further comprising~~ wherein the setting comprises ~~generating the set signal by~~ arbitrating between ~~two components on the bus~~the first and second devices.

32. (Currently amended) The method of claim 30 ~~further comprising generating the set signal by receiving a selection signal from~~ wherein the setting comprises setting the first frequency band by a user.

33. (Currently amended) The method of claim 27 wherein the second device comprises memory and wherein the method comprises:

transmitting ~~the~~a first signal ~~includes requesting memory~~to request data from ~~a~~the memory; and

~~transmitting the second signal includes returning memory~~receiving a second signal to receive requested data from ~~a~~the memory.

34. (New) The system of claim 1 wherein the second device has a receiver to receive first signals over the one line of the bus while second signals are transmitted over the one line of the bus.

35. (New) The device of claim 15, wherein the functional portion is a processor.

36. (New) The device of claim 15, wherein the functional portion is memory.

37. (New) The device of claim 15, wherein the functional portion is a controller for a chipset.

38. (New) The device of claim 15, wherein the transmitter, receiver, and functional portion are part of a single chip.

39. (New) The device of claim 17, wherein the encoder has a defined run length.

40. (New) The device of claim 17, wherein the encoder comprises a combinational logic table.

41. (New) The device of claim 15, comprising an arbitration module to set the first frequency band.